(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 100 124 A1

(12) EUROPEAN PATENT APPLICATION

published in accordance with Art. 158(3) EPC

(43) Date of publication:
16.05.2001 Bulletin 2001/20

(21) Application number: **99957663.0**

(22) Date of filing: **22.06.1999**

(51) Int. Cl.[7]: **H01L 21/76**

(86) International application number:
PCT/JP99/03297

(87) International publication number:
WO 00/01009 (06.01.2000 Gazette 2000/01)

(84) Designated Contracting States:
DE

(30) Priority: **26.06.1998 JP 18108498**
26.06.1998 JP 18108598

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(54) DIELECTRIC SEPARATION WAFER AND PRODUCTION METHOD THEREOF

(57) In a photolithography process in which a resist film 12 having window 12a is provided on the surface of silicon wafer 10 during the production of a dielectric isolated wafer, after coating back surface resist 12A onto silicon wafer 10, its entire surface is exposed to light to crosslink the entire back surface resist 12A. Consequently, during development and rinsing to avoid flooding of window 12a by back surface resist 12A that has moved around to the front side of the wafer following coating of back surface resist 12A, dissolving of the periphery of back surface resist 12A by that developing solution can be prevented. In addition, after polishing the surface of a dielectric isolated wafer on which dielectric isolated silicon island 10A is formed, low-temperature polysilicon is deposited by CVD, or SOG is coated and baked, onto the surface of the dielectric isolated wafer. As a result, depression 16a that has formed during surface polishing of the dielectric isolated wafer is filled in by low-temperature polysilicon layer 30 or the SOG layer. Next, this low-temperature polysilicon layer 30 or SOG layer is removed from the surface by polishing. At this time, the filled in portion of depression 16a on the wafer surface remains. As a result, the surface of the dielectric isolated wafer can be flattened.

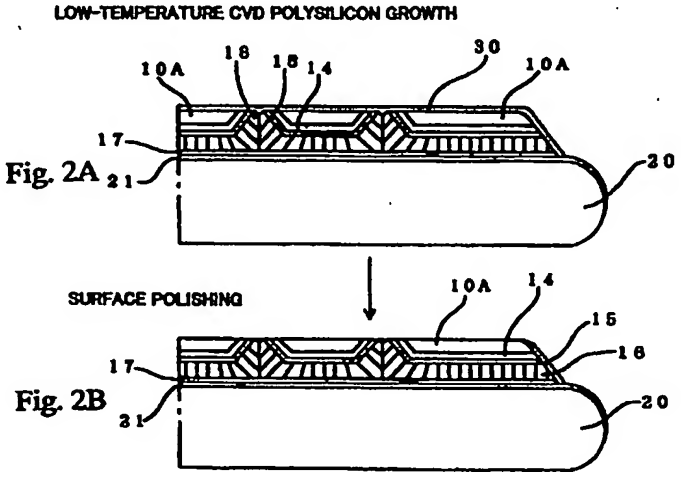

Fig. 2A

Fig. 2B

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Description

TECHNICAL FIELD

[0001] The present invention relates to a dielectric isolated wafer and its production process. More specifically, the present invention relates to the production method of a dielectric isolated wafer that prevents negative resist coated on the back surface of a silicon wafer from moving around to the front surface of the wafer periphery, and flooding the window of the groove for dielectric isolation formed in the negative resist on the wafer front surface present in this region, and when developing the surface negative resist film after coating this negative resist on the back surface, the vicinity of the periphery of the lower negative resist film is less susceptible to dissolution even if the developing solution moves around to the wafer back surface.

[0002] In addition, the present invention also relates to a dielectric isolated wafer and its production method that flattens depressions (level differences) in the wafer front surface that have formed due to separation polishing of a silicon island of a dielectric isolated wafer during production of a dielectric isolated wafer having a dielectric isolated silicon island.

[0003] Furthermore, the present application is based on Japanese Patent Application No. Hei 10-181084 and Japanese Patent Application No. Hei 10-181085, the contents of which are incorporated herein by reference.

BACKGROUND ART

[0004] Typical dielectric isolated wafers are produced by forming a groove for dielectric isolation on the surface of a silicon wafer, laminating a dielectric isolated oxide film on top of it, growing a polysilicon layer on the dielectric isolated oxide film to a thickness roughly equal to the thickness of the wafer by high-temperature chemical vapor deposition (CVD), and producing silicon single crystal of the dielectric isolated silicon island by grinding and polishing from the silicon wafer side.

[0005] However, in the case of dielectric isolated wafers produced by this method, wafers were only able to be produced up to a diameter of 4 inches due to considerations for total thickness and warping. Therefore, in order to solve problems encountered when trying to increase the diameter of these wafers, a laminated dielectric isolated wafer has recently been developed that is produced by laminating a dielectric isolated layer in the form of an active layer and a supporting substrate wafer that supports it.

[0006] This laminated dielectric isolated wafer is produced by going through each of the steps in the explanatory drawing of Fig. 5 that shows the production process of typical laminated dielectric isolated wafers. The following provides an explanation of this laminated dielectric isolated wafer with reference to Fig. 5.

[0007] To begin with, a silicon wafer 10, the surface of which is mirrored, is prepared for use as the active layer wafer (see Fig. 5A). Next, mask oxide film 11 is formed on the front and back surfaces of this silicon wafer 10 (see Fig. 5B), after which negative resist film 12 with window 12a is formed by photolithography. A window of a prescribed pattern is formed in oxide film 11 by means of this window to expose the upper layer of silicon wafer 10. Next, this silicon wafer 10 is immersed in etching solution (isopropyl alcohol (IPA)/KOH/H_2O) to perform anisotropic etching of the inside of window 12a of the wafer front surface (see Fig. 5C). As a result, dielectric isolation groove 13 having a V-shaped cross-section is formed in the wafer front surface. Furthermore, the anisotropic etching mentioned here refers to etching originating in the azimuth of the crystal surface of silicon wafer 10 in which the etching speed in the direction of depth is greater than that in the horizontal direction, and the etching speed is direction-dependent.

[0008] Next, negative resist film 12 is removed and the exposed mask oxide film 11 is washed and removed with dilute HF solution (see Fig. 5D). Subsequently, a dopant (such as Sb or As) can be thermally dispersed or ion injected into silicon wafer 10 as necessary. Dielectric isolated oxide film 14 is then formed by oxidizing heat treatment on the wafer front surface (see Fig. 5E). As a result, dielectric isolated oxide film 14 is also formed on dielectric isolation groove 13. Next, the front surface of this wafer is washed.

[0009] Subsequently, a seed amorphous silicon layer or seed polysilicon layer 15 is deposited on the front surface of silicon wafer 10 by low-temperature chemical vapor deposition (CVD) at about 600°C (about 550-700°C). After washing, high-temperature polysilicon layer 16 is grown to a thick layer on this seed amorphous silicon or seed polysilicon layer 15 by high-temperature CVD at about 1250°C (about 1200-1300°C) (see Fig. 5F). Next, the wafer periphery is chamfered, and the wafer back surface is flattened as necessary. Next, the high-temperature polysilicon layer on the front surface of the wafer is ground and polished to a thickness of 10-80 μm, and preferably 20-50 μm (see Fig. 5G). Subsequently, a low-temperature amorphous silicon layer or polysilicon layer 17 is formed to a thickness of about 1-5 μm, and preferably about 2-3 μm, by low-temperature CVD at about 600°C (550-700°C) on the front surface of the wafer, followed by polishing the low-temperature amorphous silicon layer or polysilicon layer 17 for the purpose of mirroring the laminated surfaces.

[0010] On the other hand, a silicon wafer 20 to serve as the supporting substrate wafer (which is covered by silicon oxide film 21 here) is prepared (see Fig. 5H). The front surface of this wafer is also mirrored. Next, silicon wafer 10 for the above active layer wafer is laminated onto silicon wafer 20 by contacting their respective mirrored surfaces (see Fig. 5I). Next, heat treatment is performed to increase the lamination

strength of the laminated wafer. Next, as shown in Fig. 5J, the periphery of this silicon wafer 10 for the active layer is chamfered, and after removing oxide film 21 of silicon wafer 20 for the supporting substrate by washing with HF as necessary, silicon wafer 10 for the active layer is ground and polished.

[0011] Furthermore, the amount grounded of this silicon layer 10 for the active layer is the amount at which dielectric isolated oxide film 14 is exposed to the outside, dielectric isolated silicon island 10A appears on the front surface of high-temperature polysilicon layer 16 partitioned by dielectric isolated oxide film 14, and adjacent silicon islands are completely separated. A laminated dielectric isolated wafer is produced in this manner.

[0012] However, photolithography is employed to form window 12a for anisotropic etching of dielectric isolation groove 13 in negative resist film 12 of silicon wafer 10 as previously mentioned.

[0013] Photolithography refers to a method for writing a pattern onto the front surface of negative resist film 12 coated onto silicon wafer 10 by exposure to light, followed by development. The following provides an explanation of the flow of the photolithography process while referring to the explanatory drawing of a typical photolithography process of Fig. 6.

[0014] To begin with, negative resist 12 is coated onto the front surface of silicon wafer 10 on which is formed mask oxide film 11 (see Fig. 6A), after which the solvent in negative resist film 12 is effectively removed following coating by pre-baking. Next, negative resist layer 12 is exposed to light, developed and rinsed (see Fig. 6B). Consequently, window 12a for anisotropic etching is formed in negative resist film 12 on the front surface of the wafer. Furthermore, post-baking may be performed after this in which silicon wafer 10 is loaded into a baking oven following this to promote a crosslinking reaction of surface negative resist film 12 and make it harder. Next, negative resist 12A is coated onto the back surface of the wafer to prevent dissolution of the lower side of mask oxide film 11 covering silicon wafer 10 by etching solution during anisotropic etching of a later step. More specifically, after turning over silicon wafer 10 and coating negative resist 12A onto the wafer back surface (see Fig. 6C), the wafer is loaded into a baking oven, and upper and lower negative resist films 12 and 12A are post-baked to promote a crosslinking reaction of negative resist films 12 and 12A (see Fig. 6D).

[0015] In addition, in this typical method, when negative resist 12A is coated onto the back surface of silicon wafer 10, there was the risk of this back surface negative resist 12A moving around to the front surface of the wafer periphery and flooding window 12a of groove 13 for dielectric isolation formed in front surface negative resist film 12 present in this region (see Figs. 6C and D). Therefore, a means of the prior art has been developed to resolve this problem.

[0016] Namely, after coating negative resist 12A onto the back surface of silicon wafer 10, as shown in Fig. 7C of the explanatory drawing of the lithography process pertaining to the means of the prior art of Fig. 7, silicon wafer 10 is again turned right side up, developing and rinsing treatment are performed from the front side of the wafer, and a portion of back surface negative resist 12A adhered in this window 12a is removed by washing. Furthermore, the work process performed for the other steps in Fig. 7 (Figs. 7A through 7D) is the same as that of each of the corresponding steps of Figs. 6A through 6D.

[0017] However, according to this production process of dielectric isolated wafers of the prior art, when the second round of development and rinsing treatment is performed on the front surface of the wafer shown in Fig. 7C1 in order to eliminate flooding of window 12a by a portion of back surface negative resist 12A that has moved around to the front surface of the wafer, opposite from the movement of back surface negative resist 12A to the front side shown in Fig. 7C, this second round of developing solution ends up moving around to the back side of silicon wafer 10. As a result, the periphery of unexposed back surface negative resist 12A is dissolved by this second round of developing solution, resulting in the problem of the formation of saw tooth-shaped irregularities in the periphery of silicon wafer 10 by way of these dissolved portions during anisotropic etching. These wafer caused cracking of the wafer during wafer handling, as well as cracking and chipping in the following high-temperature polysilicon formation step.

[0018] In addition, according to this production method of dielectric isolated wafers of the prior art, the upper surface of wafer 10 for the active layer is ground in the finishing step of laminated dielectric isolated wafers, and the ground surface is then polished using an alkaline polishing agent until dielectric isolated silicon island (SI island) 10A partitioned with dielectric isolated oxide film 14 is exposed.

[0019] At this time, as shown in Fig. 8, depression 16a forms on the polished front surface of active layer wafer 10 due to differences in the polishing speeds of layers 10A, 14 and 16 respectively composing this surface. In particular, at the grain boundary where high-temperature polysilicon layers 16 meet that have grown along V-shaped dielectric isolated oxide film 14, the speed at which etching progresses is greater than the other dielectric isolated silicon island 10A and dielectric isolated oxide film 14, that may also result in the formation of depression 16a having a depth of about 0.3 μm.

[0020] When a deep depression is formed in this manner, in, for example, the photolithography process during production of a device by a user following product shipment, this depression hinders uniform coating of resist onto the wafer surface, causes problems such as the occurrence of circuit disconnection or inferior resolution, and during removal of the resist film after expo-

sure, results in the risk of a portion of the film being left on the wafer surface. In addition, in other processes as well, depression 16a serves as a location for adsorption of debris. Moreover, there was also the problem of debris having been adsorbed to depression 16a normally being unable to be removed easily due to the narrow width of depression 16a.

DISCLOSURE OF THE INVENTION

[0021] The inventor of the present invention found that, if a back surface negative resist is coated onto a silicon wafer followed by exposing the entire surface to light in advance to induce a crosslinking reaction of the entire back surface negative resist film, even if developing solution moves around to the back side of the wafer during development of the front surface negative resist after coating the back surface negative resist, the periphery of this back surface negative resist film is not dissolved, thereby leading to the completion of the first invention of the present application.

[0022] The object of this first invention is to provide a production method of a dielectric isolated wafer that is able to prevent dissolution of the periphery of a negative resist film coated onto the back side of a wafer by developing solution during development treatment of a front surface negative resist after coating a back surface negative resist in a photolithography process.

[0023] In addition, another object of this first invention is to prevent partial damage of a negative resist film on the back side in the production method of a laminated dielectric isolated wafer.

[0024] This first invention is a production method of a dielectric isolated wafer in which, by covering the front and back surfaces of a silicon wafer with a mask oxide film, providing a windowed resist film on the upper surface of this mask oxide film, and masking this resist film to form a window of a prescribed pattern in the mask oxide film, a portion of the front surface of the silicon wafer is exposed through this window, a dielectric isolation groove is formed by anisotropic etching of a portion of this exposed silicon wafer front surface, a dielectric isolated oxide film is formed on the front surface of the silicon wafer, a polysilicon layer is grown on this dielectric isolated oxide film, the silicon wafer is ground and polished from the back side, and a silicon island is exposed on the polished surface that is separated by the dielectric isolated oxide film; wherein the above process of providing a windowed resist film comprises a step in which a window of a prescribed pattern is formed in this negative resist film, a step in which a negative resist is coated onto the mask oxide film of the back side, a step in which the entire surface of this negative resist film on the back side is exposed to light, and a step in which back surface negative resist adhered in the window of the front surface negative resist is removed.

[0025] High-temperature CVD is an example of a method for growing the polysilicon layer. This method consists of introducing a feed gas containing silicon into a reaction oven along with a carrier gas (such as H_2 gas), and precipitating the silicon that has formed by thermal decomposition or reduction of the feed gas on a silicon wafer heated to a high temperature. Examples of compounds containing silicon that are normally used include $SiCl_4$ and $SiHCl_3$.

[0026] An example of the reaction oven is a vertical (pancake) oven that is heated by high-frequency induction into which gas is introduced while rotating a susceptor on which a silicon wafer is placed in a dome-shaped quartz bell jar. Moreover, another type of oven that is used is a cylinder (barrel) oven in which silicon wafers are attached to each surface of a hexagonal column-shaped susceptor housed in a quartz container, followed by rotating this susceptor while introducing gas and heating with an infrared lamp.

[0027] The polysilicon growth temperature varies according to the heating system of the oven. In the case of a typical vertical oven used most commonly for this application, a growth temperature of 1200-1290°C is preferable, and that of 1230-1280°C is particularly preferable. If the growth temperature is below 1200°C, the problem results in which the wafer is susceptible to cracking. In addition, if the growth temperature exceeds 1290°C, slipping occurs which also results in the problem of the silicon wafer being susceptible to cracking.

[0028] The thickness of the polysilicon layer is the thickness resulting from adding the thickness of the polysilicon layer desired to remain to a thickness equal to two to three times the depth at which anisotropic etching was performed. If the thickness of the polysilicon layer is less than twice the depth at which anisotropic etching was performed, the groove of anisotropic etching is not adequately filled in. On the other hand, if the thickness of the polysilicon layer is greater than three times the depth at which anisotropic etching was performed, the layer ends up being deposited unnecessarily thick making this uneconomical.

[0029] In addition, in the case of forming a diffusion layer on an active layer wafer, carelessly extending thermal hysteresis is unsuitable because it significantly changes the diffusion profile.

[0030] Examples of anisotropic etching solutions that can be used include KOH (IPA/KOH/H_2O), KOH (KOH/H_2O), KOH (hydrazine/KOH/H_2O and other alkaline etching solutions. Ordinary conditions can be used for anisotropic etching conditions.

[0031] In addition, typical conditions can also be employed for the conditions of each step for forming the window for anisotropic etching in the negative resist film on the wafer front surface.

[0032] Moreover, ordinary exposure conditions can be employed for the conditions under which the entire back surface negative resist film is exposed to light, which is one of the characteristics of the present invention.

[0033] In the production method of a dielectric isolated wafer according to a first invention of the present application, the above dielectric isolated wafer may be a laminated dielectric isolated wafer produced by laminating the above active layer wafer in which a dielectric isolated silicon island is formed, and its supporting substrate wafer.

[0034] According to this first invention, mask oxide films are formed on both the front and back surfaces of the silicon wafer.

[0035] Next, a windowed negative resist film is formed on the front surface of this silicon wafer. Namely, a negative resist is coated onto the front surface of the silicon wafer, and a prescribed pattern is exposed on a mask oxide film using this negative resist film as a mask. Furthermore, development and rinsing treatment followed by post-masking may also be performed following exposure.

[0036] Subsequently, the silicon wafer is turned over and a negative resist is coated onto the wafer back surface of the mask oxide film.

[0037] Next, a crosslinking reaction is allowed to proceed over the entire back surface negative resist film by exposing the entire surface of this back surface negative resist film to light. As a result, chemical resistance to the developing solution is imparted to the back surface negative resist film.

[0038] Next, the silicon wafer is turned right side up and developing treatment is performed on the front surface negative resist film after exposure. Furthermore, in the front surface negative resist film is to be developed immediately after exposure, this development consists of a second round of developing treatment to avoid flooding of the window caused by back surface negative resist that has come around to the front of the wafer.

[0039] At this time, even if developing solution comes around to the back of the silicon wafer and adheres to the periphery of the back surface negative resist, there is hardly any risk of this portion being dissolved. This is because the back surface negative resist film has been given enhanced chemical resistance by full surface exposure.

[0040] Subsequently, this silicon wafer, which has been covered by front and back negative resist films, is immersed in etching solution, and anisotropic etching is performed on the portion of the silicon wafer inside of the mask oxide film and this film through the window in the wafer front surface. As a result, a dielectric isolation groove is formed.

[0041] Next, the negative resist films of the front and back surfaces along with the mask oxide film are removed.

[0042] A dielectric isolated oxide film is then formed on the front surface of the wafer by oxidizing heat treatment.

[0043] Subsequently, after growing polysilicon on this dielectric isolated oxide film, the silicon wafer is ground and polished from the back of the wafer resulting in the appearance of the dielectric isolated silicon island. Thus, a dielectric isolated wafer is produced in this manner.

[0044] In the case the dielectric isolated wafer is a laminated dielectric isolated wafer as previously mentioned in particular, the produced active layer wafer having a dielectric isolated silicon island made of polysilicon and its supporting substrate wafer are laminated to produce a laminated dielectric isolated wafer having the effect of the present invention. As a result, the present invention can be applied to laminated dielectric isolated wafers for which there is little risk of decreased quality of the dielectric isolated silicon island due to thermal decomposition caused by high-temperature CVD.

[0045] In addition, the inventors of the present invention noticed that various problems that occur during device production by a user as previously described as a result of either depositing (growing) polysilicon on the front surface of a wafer or baking SOG (spin-on-glass) after coating following surface polishing of a dielectric isolated wafer are resolved if the polysilicon layer or SOG layer is removed by polishing while leaving a portion in which depressions in the wafer surface are filled in, thereby leading to completion of the second invention of the present application.

[0046] The object of this second invention is to provide a dielectric isolated wafer and its production method in which the surface of the dielectric isolated wafer is flattened.

[0047] In addition, another object of this second invention is to provide a dielectric isolated wafer and its production method that is no occurrence of quality deterioration of the silicon island during adherence of an embedded polysilicon layer.

[0048] Moreover, still another object of this second invention is to provide a production method of a dielectric isolated wafer for which there is little risk of depressions in the wafer surface reforming during removal of a polysilicon layer by polishing.

[0049] The dielectric isolated wafer according to this second invention is a dielectric isolated wafer comprising polishing the front surface of a dielectric isolated wafer on which a dielectric isolated silicon island has been formed, and then forming a polysilicon layer on the front surface of this dielectric isolated wafer by CVD, as a result of which depressions in the wafer surface that formed during surface polishing of the above dielectric isolated wafer are filled in, after which the polysilicon layer is removed by polishing while leaving a portion in which the above depressions are filled in.

[0050] CVD for forming the polysilicon layer refers to a method in which a feed gas containing silicon is introduced into a reaction oven along with a diluting gas (normally N2 gas) to precipitate silicon formed by thermal decomposition or reduction of the feed gas on a silicon wafer heated to a high temperature. Examples of silicon-containing compounds that are used include

SiH_2Cl_2 and SiH_4. Examples of CVD methods include high-temperature CVD and low-temperature CVD.

[0051] An example of a reaction oven is a horizontal oven in which, for example, a silicon wafer on a boat fixed inside a horizontally long quartz tube is resistance-heated while introducing a gas. In addition, another example of a reaction oven is a vertical oven in which gas is introduced while rotating a vertical quartz (SiC) boat on which is placed a silicon wafer in a bell-shaped quartz (SiC) bell jar followed by high-frequency induction heating.

[0052] The thickness of the amorphous silicon layer or polysilicon layer deposited (grown) by CVD is preferably 0.2-5 μm, and particularly preferably 0.4-1.0 μm. If the thickness is less than 0.2 μm, the problem results in which the level differences in the surface are not adequately eliminated. In addition, if the thickness exceeds 5 μm, the problem results in which the amount of time for flattening polishing becomes unnecessarily long.

[0053] Examples of polishing liquids used during surface polishing of the dielectric isolated wafer include those in which polishing grit (SiO_2) having a mean particle size of 10-100 nm is added at 3-4 wt% to an alkaline etching solutions such as NaOH or KOH.

[0054] The amount of polysilicon layer polished is the amount that allows the polysilicon layer to be removed while leaving the portion at which depressions formed in the surface of the dielectric isolated water are filled in.

[0055] The above dielectric isolated wafer may also be a laminated wafer in which an active layer wafer, in which a dielectric isolated silicon island is formed in the front surface, and a supporting substrate wafer, are laminated. Commonly known wafer lamination technologies can be employed for this lamination.

[0056] In addition, this production method of a dielectric isolated wafer according to this second invention comprises polishing the surface of a dielectric isolated wafer in which is formed a dielectric isolated silicon island followed by the formation of a polysilicon layer by CVD on the front surface of this dielectric isolated wafer, said method comprising a step in which depressions in the wafer surface that were formed during surface polishing of the above dielectric isolated wafer are filled in, and a step in which the polysilicon layer is removed by polishing while leaving the portion at which the above depressions are filled in.

[0057] Here, the description relating to the dielectric isolated wafer according to the above second invention also applies to this production method of a dielectric isolated wafer.

[0058] Furthermore, examples of methods that can be used for forming the amorphous silicon layer or polysilicon layer include reduced pressure CVD and normal pressure CVD. The pressure during film deposition by reduced pressure CVD is about 10-80 Pa.

[0059] In the production method of a dielectric isolated wafer according to this second invention, the polysilicon layer for filling in the above depressions may be formed by low-temperature CVD at 550-700°C.

[0060] If the temperature is lower than 550°C, the problem results in which the deposition rate slow down. In addition, if the temperature exceeds 700°C, the polysilicon particles become larger resulting in the problem of increased difficulty in flattening during later flattening polishing.

[0061] In addition, the pressure during film deposition by this low-temperature CVD is 10-80 Pa when performed by reduced pressure CVD or normal pressure when performed by normal pressure CVD.

[0062] In addition, another form of a dielectric isolated wafer according to the second invention is a dielectric isolated wafer for which, after polishing the surface of a dielectric isolated wafer on which a dielectric isolated silicon island has been formed, by forming an SOG layer on the surface of this dielectric isolated wafer, depressions in the wafer surface that form during surface polishing of the above dielectric isolated wafer are filled in, after which the SOG layer is removed by polishing while leaving the above filled in portion of the depressions.

[0063] An example of a method for coating SOG (ethyl silicate) involves performing spin coating while rotating the dielectric isolated wafer.

[0064] In addition, another form of the production method of a dielectric isolated wafer according to the second invention is a production method of a dielectric isolated wafer by polishing the surface of a dielectric isolated wafer on which is formed a dielectric isolated silicon island followed by forming an SOG layer by coating SOG onto the surface of this dielectric isolated wafer and baking, comprising a step wherein depressions in the wafer surface that occur during surface polishing are filled in, and a step wherein this SOG layer is removed by polishing while leaving the above filled in portion of the depressions.

[0065] The coating thickness of SOG is preferably 0.2-2.0 μm, and particularly preferably 0.3-0.6 μm. If the coating thickness is less than 0.2 μm, the above filling in of the depressions is inadequate. In addition, if the coating thickness exceeds 2.0 μm, over-coating is required in the SOG coating method resulting in the problem of increased susceptibility to uneven thickness.

[0066] SOG baking is performed in the N_2 gas atmosphere in a harness and so forth to vaporize the alcohol content in the SOG. The baking temperature is 200-250°C. If the baking temperature is lower than 200°C, the problem occurs in which a long period of time is required to vaporize the alcohol content in the SOG. In addition, if the baking temperature exceeds 250°C, although there is no particular problem provided the temperature is not so high as to cause significant diffusion of the dopant present (e.g., 900°C or higher), the use of this high a temperature is not required. The SOG baking time is 30-60 minutes.

[0067] According to this second invention, after pol-

ishing the surface of a dielectric isolated wafer on which has been formed a dielectric isolated silicon island, a polysilicon layer is deposited (grown) by CVD, or an SOG layer is formed by coating with SOG and baking, onto the surface of the dielectric isolated wafer. When this is done, depressions formed during surface polishing of the dielectric isolated wafer are filled in by the polysilicon layer or SOG layer. Next, this polysilicon layer or SOG layer is removed by polishing the surface. At this time, polishing is performed while leaving behind the filled in portion of the depressions on the wafer surface. As a result, the surface of the dielectric isolated wafer can be flattened.

[0068] In particular, this second invention can also be applied to a laminated dielectric isolated wafer as previously mentioned. Accordingly, in the case of comparing with the production method of a dielectric isolated wafer in a non-laminated method, since warping of the wafer can be held to a low level, the present invention can also be applied to large-diameter wafers measuring 5 inches or more in diameter.

[0069] Moreover, in the case the polysilicon layer for filling in the depressions in the production method of a dielectric isolated wafer as described above is a low-temperature amorphous silicon layer or polysilicon layer formed by low-temperature CVD at 550-700°C, it has smaller crystal particles as compared with a high-temperature polysilicon layer, thereby reducing the risk of depressions in the wafer surface reforming during removal of the polysilicon layer by polishing.

[0070] Furthermore, it is also possible to carry out the present invention by combining the above first and second inventions. In this case, both the effects of the above first and second inventions are demonstrated.

BRIEF DESCRIPTION OF THE DRAWINGS

[0071]

Fig. 1 is an explanatory drawing showing a photolithography process in the production method of the dielectric isolated wafer according to a first embodiment of the present invention.

Fig. 2 is an explanatory drawing showing a production process of a laminated dielectric isolated wafer as claimed in a third embodiment of the present invention.

Fig. 3 is an enlarged cross-sectional drawing of the essential portion of a laminated dielectric isolated wafer produced by the production method of the dielectric isolated wafer according to a third embodiment of the present invention.

Fig. 4 is an explanatory drawing showing a production process of a laminated dielectric isolated wafer according to a fourth embodiment of the present invention.

Fig. 5 is an explanatory drawing showing a production process of a typical laminated dielectric isolated wafer.

Fig. 6 is an explanatory drawing of a typical photolithography process.

Fig. 7 is an explanatory drawing of a photolithography process according to the prior art.

Fig. 8 is an enlarged cross-sectional drawing of the essential portion of a laminated dielectric isolated wafer produced according to the prior art.

BEST MODE FOR CARRYING OUT THE INVENTION

[0072] The following provides an explanation of the production method of a dielectric isolated wafer as claimed in the embodiments of the present invention. Furthermore, this explanation uses the example of a laminated dielectric isolated wafer explained as an example of the prior art previously described. Thus, the same reference numerals are used for those constituents that are the same as those shown in Figs. 5 through 8. Reference symbol 10 is a silicon wafer for the active layer wafer, reference symbol 10A is a dielectric isolated silicon island, reference symbol 11 is a mask oxide film, reference symbol 12 is a negative resist film, reference symbol 12a is a window, reference symbol 13 is a dielectric isolation groove, reference symbol 14 is a dielectric isolated oxide film, reference symbol 16 is polysilicon, reference symbol 16a is a depression, reference symbol 20 is a silicon wafer for the supporting substrate wafer, reference symbol 30 is a low-temperature polysilicon layer (polysilicon layer), and reference symbol 300 is an SOG layer.

[0073] Fig. 1 is an explanatory drawing showing a photolithography process of the production method of a dielectric isolated wafer as claimed in a first embodiment of the present invention. The basic process of the production method of the dielectric isolated wafer of this first embodiment of the present invention is the same as the production process of a typical laminated dielectric isolated wafer shown in Figs. 5 and 7 explained in the section on the prior art. In the present invention, however, a portion of the basic photolithography process during production of the dielectric isolated wafer shown in Fig. 7 differs from the case of the prior art.

[0074] To begin with, a silicon wafer 10 is obtained for which the front and back surfaces have been mirrored to serve as the active layer wafer (see Fig. 5A).

[0075] Next, mask oxide film 11 is formed on the front and back surfaces of this silicon waver 10 (see Fig. 5B).

[0076] Next, negative resist film 12 with window 12a is formed by photolithography.

[0077] Next, silicon wafer 10 is immersed in etching solution ($IPA/KOH/H_2O$) to perform anisotropic etching of the wafer surface (see Fig. 5C). As a result, groove 13 for dielectric isolation having a V-shaped cross-section is formed in the wafer surface.

[0078] Next, negative resist film 12 is removed, after which the exposed mask oxide film 11 is removed

(see Fig. 5D).

[0079] Subsequently, a dopant is injected into the silicon as necessary, after which dielectric isolated oxide film 14 is formed on the wafer surface by oxidizing heat treatment (see Fig. 5E). As a result, dielectric isolated oxide film 14 is also formed on dielectric isolation groove 13.

[0080] Next, the surface of the wafer is washed.

[0081] Subsequently, seed polysilicon layer 15 is deposited by low-temperature CVD at about 600°C on the surface of silicon wafer 10.

[0082] After washing, high-temperature polysilicon layer 16 is grown to a thick layer on this seed polysilicon layer 15 by high-temperature CVD at about 1250°C (see Fig. 5F).

[0083] Next, the wafer periphery is chamfered and the back surface of the wafer is flattened as necessary. Next, high-temperature polysilicon layer 16 on the surface of the wafer is ground and polished to a thickness of about 30 μm (see Fig. 5G).

[0084] Subsequently, after forming low-temperature polysilicon layer 17 having a thickness of about 3.0 μm on the wafer surface by low-temperature CVD at 600°C, the surface of low-temperature polysilicon layer 17 is polished for the purpose of mirroring the laminated surfaces.

[0085] On the other hand, a silicon wafer 20 (which here is covered with silicon oxide film 21) is obtained to serve as a supporting substrate wafer (see Fig. 5H). The surface of the wafer is then mirrored.

[0086] Next, silicon wafer 10 for the above active layer wafer is laminated onto this silicon wafer 20 by bringing into contact the corresponding mirrored surfaces (see Fig. 5I).

[0087] Next, heat treatment is performed to enhance the lamination strength of this laminated wafer.

[0088] Next, as shown in Fig. 5J, the periphery of this silicon wafer 10 for the active layer is chamfered, and after removing oxide film 21 of silicon wafer 20 for the supporting substrate by washing with HF as necessary, silicon wafer 10 for the active layer is ground and polished. The amount of this silicon wafer 10 that is grounded is the amount at which dielectric isolated oxide film 14 is exposed to the outside, dielectric isolated silicon island 10A appears on the front surface of high-temperature polysilicon layer 16 partitioned by dielectric isolated oxide film 14, and adjacent silicon islands are completely separated.

[0089] A laminated dielectric isolated wafer is produced in this manner.

[0090] The following provides an explanation of the photolithography process in this first embodiment. To begin with, negative resist 12 is spin-coated onto the surface of silicon wafer 10 (see Fig. 1A) on which mask oxide film 11 is formed and for which the surface is held level.

[0091] Next, after going through pre-baking, exposure, development and rinsing steps normally performed in this photolithography process, window 12a of a prescribed pattern is provided in this negative resist film 12 (see Fig. 1B). Furthermore, this may be followed by placing silicon wafer 10 in a baking oven not shown to post-bake negative resist film 12 on the surface of the wafer.

[0092] Subsequently, silicon wafer 10 with window 12a is turned over and negative resist 12A is spin-coated onto the back surface of the wafer. At this time, back surface negative resist 12A moves around to the front surface of the wafer periphery and floods window 12a formed in front surface negative resist film 12 present in this region (see Fig. 1C).

[0093] Next, the entire surface of back surface negative resist 12A is exposed to light to crosslink this back surface negative resist 12A (see Fig. 1C2). This step is a characteristic of the present invention. As a result of performing this crosslinking reaction, the chemical resistance of back surface negative resist film 12A to etching solution is enhanced.

[0094] Subsequently, exposed silicon wafer 10 is turned right side up, and a second round of development and rinsing treatment is performed from the front side of the wafer. As a result, the above-mentioned back surface negative resist 12A that is flooding window 12a is removed by washing. At this time, the second round of developing solution moves around to the back side of the wafer periphery and dissolves a portion of the periphery of back surface negative resist film 12 (see Fig. 1C1).

[0095] However, as shown in Fig. 1C2, this back surface negative resist film 12A has been crosslinked in advance by exposing the entire surface to light giving it enhanced chemical resistance. As a result, the periphery of back surface negative resist film 12A is resistant to dissolution even though it is subjected to a second round of developing solution.

[0096] Subsequently, silicon wafer 10 is placed in a baking oven and front and back surface negative resists 12 and 12A are post-baked.

[0097] In the present embodiment, since a laminated dielectric isolated wafer is used in which active layer wafer 10, having dielectric isolated silicon island 10A, and supporting substrate wafer 20 are laminated together, it is not necessary to grow the polysilicon layer to a thick layer by high-temperature CVD.

[0098] Next, the following provides an explanation of the production method of a dielectric isolated wafer as claimed in a second embodiment of the present invention.

[0099] This production method of the dielectric isolated wafer of a second embodiment consists of sequentially coating front surface negative resist 12 onto the surface of silicon wafer 10 of Fig. 1B in the production method of the first embodiment, followed by turning over silicon wafer 10 without developing or rinsing front surface negative resist film 12 so that the back side of the wafer is facing up. After then coating back

surface negative resist 12 onto the back side of this wafer, the entire surface of this film 12 is exposed to light. Next, silicon wafer is turned right side up, front surface negative resist film 12 is developed and rinsed to form window 12a, and front and back surface negative resist films 12 and 12A are post-baked.

[0100] In this second embodiment, development treatment of front surface negative resist film 12 does not have to be performed twice as in the first embodiment, but only needs to be performed once. As a result, the number of production steps of the dielectric isolated wafer can be reduced.

[0101] Next, the following provides an explanation of a dielectric isolated wafer and its production method as claimed in a third embodiment of the present invention.

[0102] To begin with, a silicon wafer is produced and obtained having mirrored front surface to serve as the active layer wafer (see Fig. 5A).

[0103] Next, mask oxide film 11 is formed on the surface of this silicon wafer 10 (see Fig. 5B).

[0104] Next, resist film 12 is adhered to oxide film 11. A window of a prescribed pattern is then formed in this resist film 12.

[0105] Subsequently, a window having the same pattern is formed in oxide film 11 through this window, and a portion of the surface of silicon wafer 10 is exposed.

[0106] Next, resist film 12 is removed.

[0107] Moreover, this silicon wafer 10 is immersed for a prescribed amount of time in etching solution ($IPA/KOH/H_2O$). As a result, a concave irregularity (depression) of a prescribed pattern is formed in the surface of the silicon wafer. Anisotropic etching is then performed on the wafer surface (Fig. 5C) resulting in the formation of dielectric isolation groove 13 having a V-shaped cross-section.

[0108] Next, mask oxide film 11 is removed by washing with a dilute HF solution (Fig. 5D). At this time, a dopant may be introduced into the silicon bulk.

[0109] Next, dielectric isolated oxide film 14 of a prescribed thickness is formed on the silicon wafer surface by oxidizing heat treatment (Fig. 5E).

[0110] The wafer surface is then washed.

[0111] Next, seed polysilicon layer 15 is deposited on the surface of this silicon wafer 10 by low-temperature CVD at about 600°C.

[0112] Moreover, after washing, high-temperature polysilicon layer 16 is grown to a prescribed thickness on this seed polysilicon layer 15 by high-temperature CVD at about 1250°C. (Fig. 5F).

[0113] Next, the periphery of the wafer is chamfered and the wafer back surface is flattened as necessary.

[0114] Next, high-temperature polysilicon layer 16 on the wafer surface is ground and polished to a thickness of 30 μm (Fig. 5G).

[0115] Alternatively, after this, low-temperature polysilicon layer 17 may be deposited to a thickness of 3 μm on the wafer surface as necessary by low-temperature CVD at 600°C followed by polishing the surface.

[0116] On the other hand, silicon wafer 20 is obtained for the supporting substrate (Fig. 5H).

[0117] Next, the above silicon wafer 10 for the active layer is laminated onto this silicon wafer 20 by aligning the corresponding mirrored surfaces (Fig. 5I).

[0118] This laminated wafer 30 is then subjected to a prescribed lamination heat treatment.

[0119] Next, as shown in Fig. 5J, the periphery of this active layer wafer side is chamfered, and after removing oxide film 21 of supporting substrate wafer 20 as necessary, the surface of the active layer wafer is ground and polished. The amount of this active layer wafer grounded is the amount at which dielectric isolated silicon island 10A partitioned by dielectric isolated oxide film 14 appears (also see Fig. 8).

[0120] Figs. 2A and B are explanatory drawings showing the production process of a laminated dielectric isolated wafer as claimed in this third embodiment of the present invention.

[0121] In this manner, a laminated dielectric isolated wafer is produced as shown in Fig. 5J. At this time, depression 16a having a depth of about 0.3 μm produced during surface polishing is formed in the surface of the active layer wafer (also see Fig. 8).

[0122] After inserting this laminated dielectric isolated wafer into a reaction oven, SiH_4, which serves as the growth gas a prescribed concentration, is introduced into the oven along with diluting gas (H_2 gas), and low-temperature polysilicon layer 30 is laminated to a thickness of 0.5 μm on the entire surface of the active layer wafer heated to 600°C by a resistance heater. Furthermore, the pressure during deposition is 50 Pa. As a result, the above depression 16a is filled in by low-temperature polysilicon layer 30 (see dotted line in Fig. 3). Fig. 2A shows this state.

[0123] Next, as shown in Fig. 2B, the surface of this polysilicon layer 30 is removed by polishing with a commonly known polishing device using NaOH solution for the polishing liquid and SiO_2 polishing grit while leaving behind only the filled in portion 30A of depression 16a. More specifically, the surface is polished until the surface of dielectric isolated silicon island 10A is exposed.

[0124] Consequently, the surface of the active layer wafer can be flattened. As a result, resist can be uniformly coated onto a wafer surface in, for example, the photolithography process during device production by a user. In addition, circuit disconnection and deterioration of resolution can be prevented during exposure of this photolithography process, and when removing the resist film after exposure, the risk of a portion of this film remaining on the wafer surface can be eliminated. In addition, the entrance of debris into this depression 16a and this serving as a site for adsorption of debris can be prevented in other processes as well.

[0125] In this manner, since a laminated dielectric isolated wafer is produced that combines an active layer

wafer, which has dielectric isolated silicon island 10A, and a supporting substrate wafer 20, high-temperature heating for an extended period of time by high-temperature CVD required in the case of not employing a lamination method is no longer necessary. In addition, warping of the dielectric isolated substrate can be held to a low level. In addition, since depression 16a is filled in by a low-temperature amorphous silicon layer or polysilicon layer 30 by low-temperature CVD at 550-700°C, the risk of depression 16a reforming on the wafer surface during removal of this low-temperature amorphous silicon layer or polysilicon layer 30 by polishing can be reduced. This is because the crystal particles of the low-temperature amorphous silicon layer or polysilicon layer are smaller than those of a high-temperature polysilicon layer.

[0126] Subsequently, the flatness of the surface of the active layer wafer of this dielectric isolated wafer was actually attempted to be measured using a contact needle type flatness gauge.

[0127] The average flatness of the surfaces of 25 active layer wafers produced according to the method of the prior art was 0.24 μm. In contrast, the average flatness in the case of employing the production method of the present invention was 0.01 μm.

[0128] Next, an explanation is provided of a dielectric isolated wafer and its production method of a fourth embodiment of the present invention based on Fig. 4. Figs. 4A-C are explanatory drawings showing the production process of a laminated dielectric isolated wafer of this fourth embodiment of the present invention.

[0129] In this fourth embodiment, an example is shown of employing a method in which SOG (ethyl silicate) is formed on the surface of the active layer wafer as a method for providing filled in portion 300A that fills depression 16a on the surface of the active layer wafer.

[0130] Namely, as shown in Fig. 4A, SOG300 is spin-coated to a thickness of 0.6 μm onto the surface of the active layer wafer. Subsequently, as shown in Fig. 4B, this SOG layer 300 is baked solid while vaporizing alcohol by a harness. This baking is performed for a baking time of 30-60 minutes and at a baking temperature of 200-250°C in an N2 gas atmosphere. Following this baking, polishing is performed to flatten the wafer surface in the same manner as low-temperature polysilicon layer 30 (see Fig. 4C).

[0131] Furthermore, in the case of using this SOG, HF treatment cannot be performed. This is because, if the wafer is immersed in HF solution, the SOG is immediately etched off to its original state. Furthermore, end-point detection of the SOG surface can be confirmed by the presence of its water breakdown.

[0132] When the average flatness of the surfaces of 25 active layer wafers produced by this SOG was measured, in contrast to flatness being 0.24 μm with the method of the prior art, favorable results of 0.02 μm were obtained.

[0133] Furthermore, although the above has provided individual explanations of each embodiment, the present invention can also be carried out by combining the first and third embodiments, first and fourth embodiments, second and third embodiments or second and fourth embodiments.

INDUSTRIAL APPLICABILITY

[0134] According the first invention, since a negative resist is coated onto the back surface of a silicon wafer followed by exposure of the entire surface to light, the periphery of the negative resist film coated on the back of the wafer can be prevented from being dissolved by developing solution during surface negative resist development treatment following coating of the back surface negative resist.

[0135] In particular, the present invention can also be applied to a laminated dielectric isolated wafer. In this case, growing a thick polysilicon layer by high-temperature CVD is not required.

[0136] According to the second invention, after polishing the surface of a dielectric isolated wafer, polysilicon is deposited (grown) by CVD or SOG is coated and then baked onto the wafer surface to fill in depressions in the wafer surface. Subsequently, since the polysilicon layer or SOG layer is then removed by polishing while leaving behind the filled in portion of the depressions, the surface of the dielectric isolated wafer can be flattened.

[0137] In particular, in the case of applying the present invention to a laminated dielectric isolated wafer, since an active layer wafer having a dielectric isolated silicon island, and a supporting substrate layer are laminated to produce a laminated dielectric isolated wafer, and depressions in the surface of this laminated dielectric isolated wafer are filled in to flatten the surface, a advantages are obtained over dielectric isolated wafers not produced by this lamination method. Namely, as a result of substituting the supporting substrate with a single crystal silicon wafer, warping of the wafer can be held to, for example, 150 μm or less even in the case of large diameter wafers measuring 5 inches or more.

[0138] Moreover, in the case of using low-temperature polysilicon formed by low-temperature CVD at 550-700°C for the polysilicon layer for filling in the depressions in the production method of a dielectric isolated wafer, the risk of the depressions reforming in the wafer surface can be reduced during removal of this polysilicon layer by polishing.

Claims

1. A production method of a dielectric isolated wafer comprising:

   covering the front and back surfaces of the silicon wafer with a mask oxide film,
   providing a windowed resist film on the surface

of this mask oxide film,
exposing a portion of the silicon wafer surface through a window by forming a window of a prescribed pattern in a mask oxide film by using this resist film as a mask,
forming a dielectric isolation groove by anisotropic etching of this exposed portion of the silicon wafer surface,
forming a dielectric isolated oxide film on the surface of the silicon wafer,
growing a polysilicon layer on this dielectric isolated oxide film, and
grinding and polishing the silicon wafer from the back side to cause a silicon island separated by a dielectric isolated oxide film to appear on the polished surface; wherein
the process of providing the above windowed resist film comprises:
a step in which a negative resist is coated onto the surface of said mask oxide film,
a step in which a window of a prescribed pattern is formed in this negative resist film,
a step in which a negative resist is coated on the mask oxide film on the back side,
a step in which the entire surface of this back side negative resist film is exposed to light, and
a step in which the back surface negative resist adhered to the window of the front surface negative resist is removed.

2. A production process of a dielectric isolated wafer according to claim 1, wherein said dielectric isolated wafer is produced by laminating an active surface layer in which said dielectric isolated silicon island is formed, and its supporting substrate layer.

3. A dielectric isolated wafer in which, by polishing the surface of a dielectric isolated wafer on which a dielectric isolated silicon island is formed, followed by forming a polysilicon layer by CVD on the surface of this dielectric isolated wafer, depressions in the wafer surface that have formed during surface polishing of said dielectric isolated wafer are filled in, after which the polysilicon layer is removed by polishing while leaving behind the filled in portion of said depressions.

4. A dielectric isolated wafer according to claim 3, wherein said dielectric isolated wafer is a laminated dielectric isolated wafer in which an active layer wafer, on the surface of which a dielectric isolated silicon island is formed, and a supporting substrate wafer are laminated.

5. A production process of a dielectric isolated wafer comprising:

a step in which, by polishing the surface of a dielectric isolated wafer on which a dielectric isolated silicon island is formed, followed by forming a polysilicon layer by CVD on the surface of this dielectric isolated wafer, depressions in the wafer surface that have formed during surface polishing of said dielectric isolated wafer are filled in, and
a step in which this polysilicon layer is removed by polishing while leaving behind the filled in portion of said depressions.

6. A production process of a dielectric isolated wafer according to claim 5, wherein said polysilicon layer for filling in said depressions is formed by low-temperature CVD at 550-700°C.

7. A dielectric isolated wafer in which, by polishing the surface of a dielectric isolated wafer on which is formed a dielectric isolated silicon island, followed by forming an SOG layer on the surface of this dielectric isolated wafer, depressions in the wafer surface that have formed during surface of polishing of said dielectric isolated wafer are filled in, after which this SOG layer is removed by polishing while leaving behind the filled in portion of said depressions.

8. A production process of a dielectric isolated wafer comprising:

a step in which, by polishing the surface of a dielectric isolated wafer on which a dielectric isolated silicon island is formed, followed by coating and baking SOG onto the surface of this dielectric isolated wafer, depressions in the wafer surface that have formed during surface polishing of said dielectric isolated wafer are filled in, and
a step in which this SOG layer is removed by polishing while leaving behind the filled in portion of said depressions.

MASK OXIDE FILM FORMATION

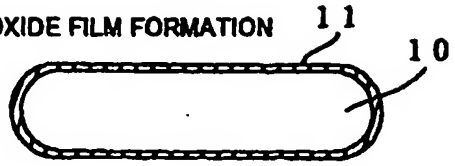


Fig. 1A

RESIST COATING → PRE-BAKING
EXPOSURE OF ENTIRE FRONT SURFACE
→ DEVELOPING AND RINSING

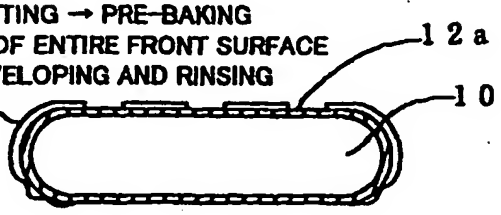


Fig. 1B

BACK SURFACE RESIST COATING

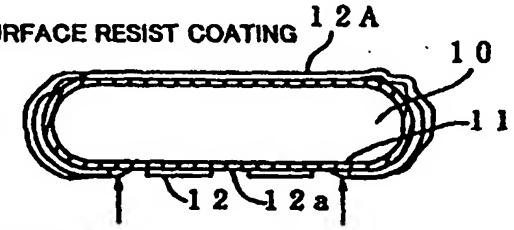


Fig. 1C

MOVEMENT AROUND WAFER
BY BACK SURFACE RESIST

EXPOSURE OF ENTIRE BACK SURFACE

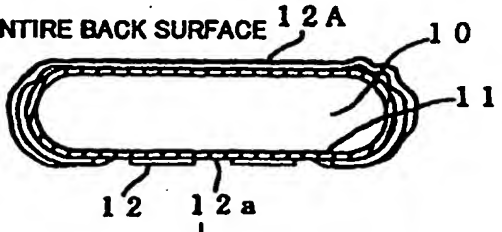


Fig. 1C2

SECOND ROUND OF DEVELOPMENT AND
RINSING FROM FRONT SIDE

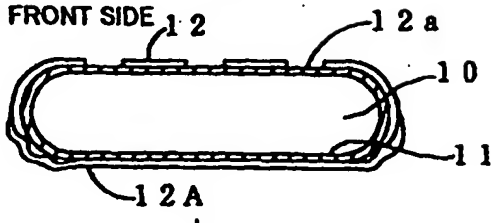


Fig. 1C1

POST-BAKING

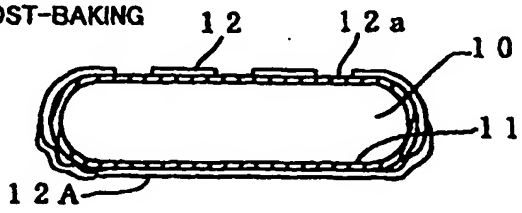


Fig. 1D

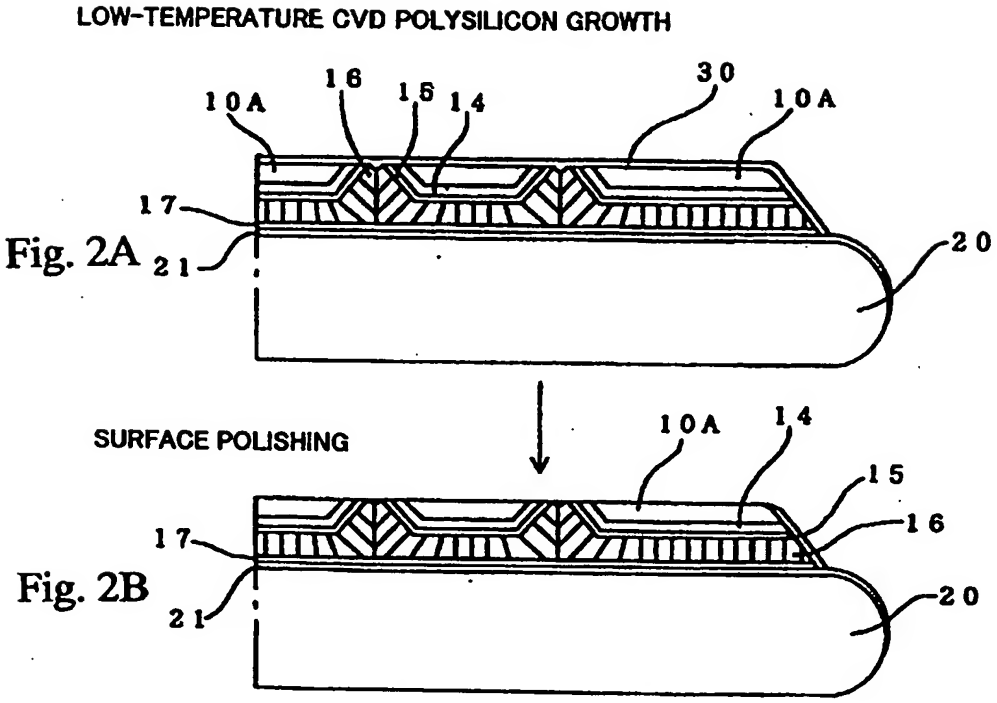
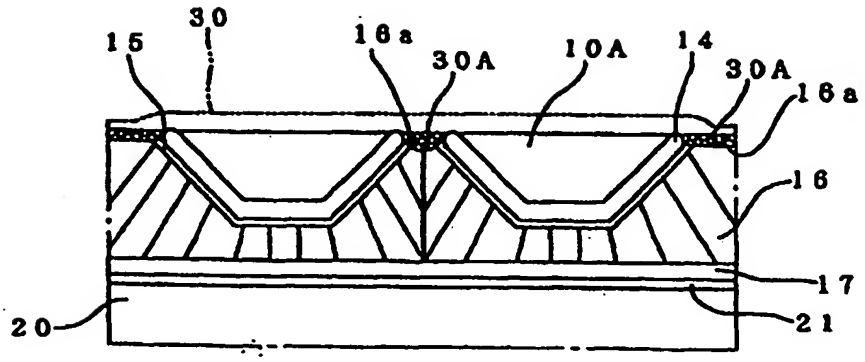

LOW-TEMPERATURE CVD POLYSILICON GROWTH
10A
16
15
14
30
10A
17
21
20

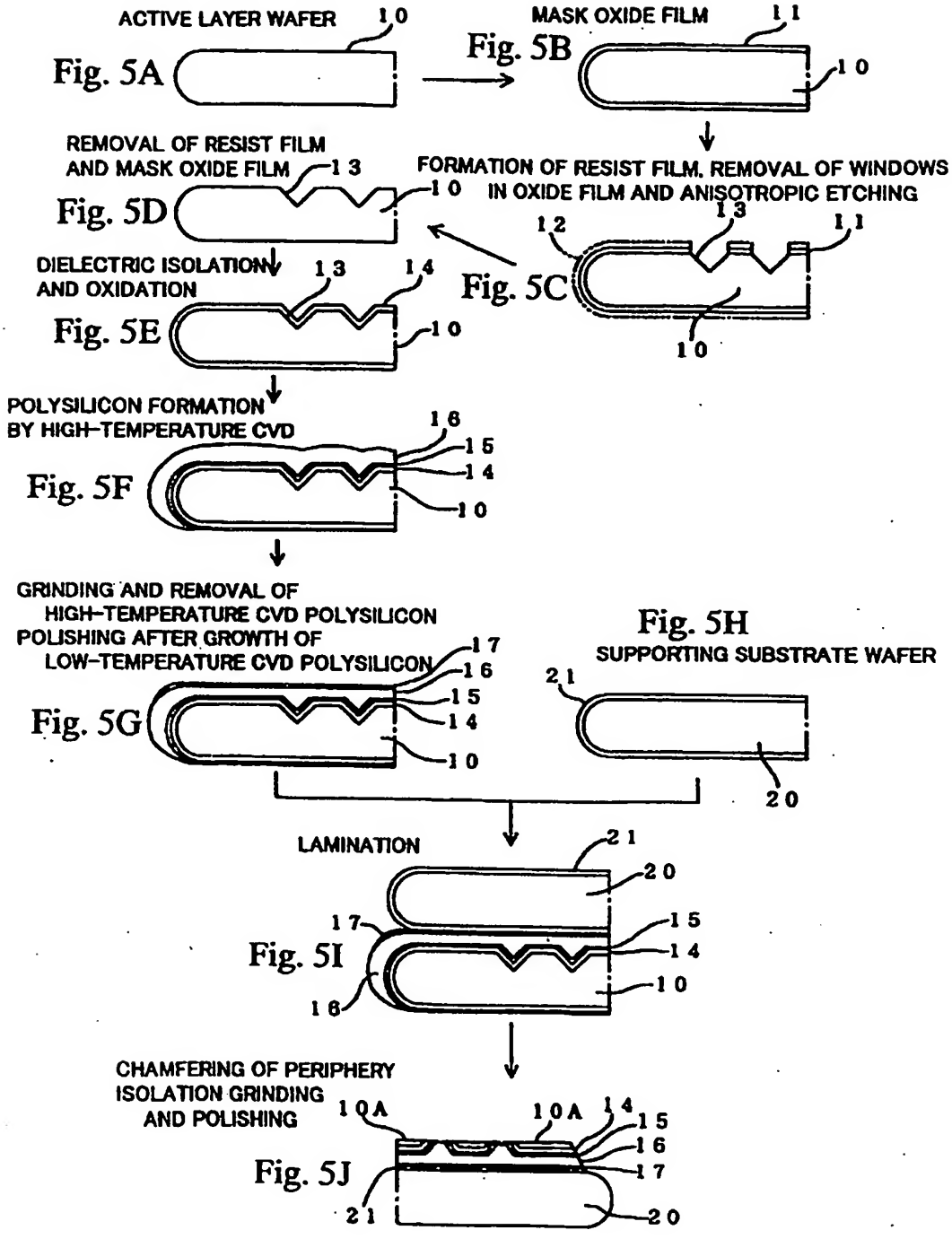
Fig. 2A

SURFACE POLISHING
10A
14
15
16
17
21
20

Fig. 2B

Fig. 3




ACTIVE LAYER WAFER
10
Fig. 5A
MASK OXIDE FILM
11
Fig. 5B
10
REMOVAL OF RESIST FILM
AND MASK OXIDE FILM
13
Fig. 5D
10
FORMATION OF RESIST FILM, REMOVAL OF WINDOWS
IN OXIDE FILM AND ANISOTROPIC ETCHING
12
13
11
Fig. 5C
10
DIELECTRIC ISOLATION
AND OXIDATION
13
14
Fig. 5E
10
POLYSILICON FORMATION
BY HIGH-TEMPERATURE CVD
16
15
14
Fig. 5F
10
GRINDING AND REMOVAL OF
HIGH-TEMPERATURE CVD POLYSILICON
POLISHING AFTER GROWTH OF
LOW-TEMPERATURE CVD POLYSILICON
17
16
15
14
Fig. 5G
10
Fig. 5H
SUPPORTING SUBSTRATE WAFER
21
20
LAMINATION
21
20
17
15
14
Fig. 5I
10
16
CHAMFERING OF PERIPHERY
ISOLATION GRINDING
AND POLISHING
10A
10A
14
15
16
17
Fig. 5J
21
20

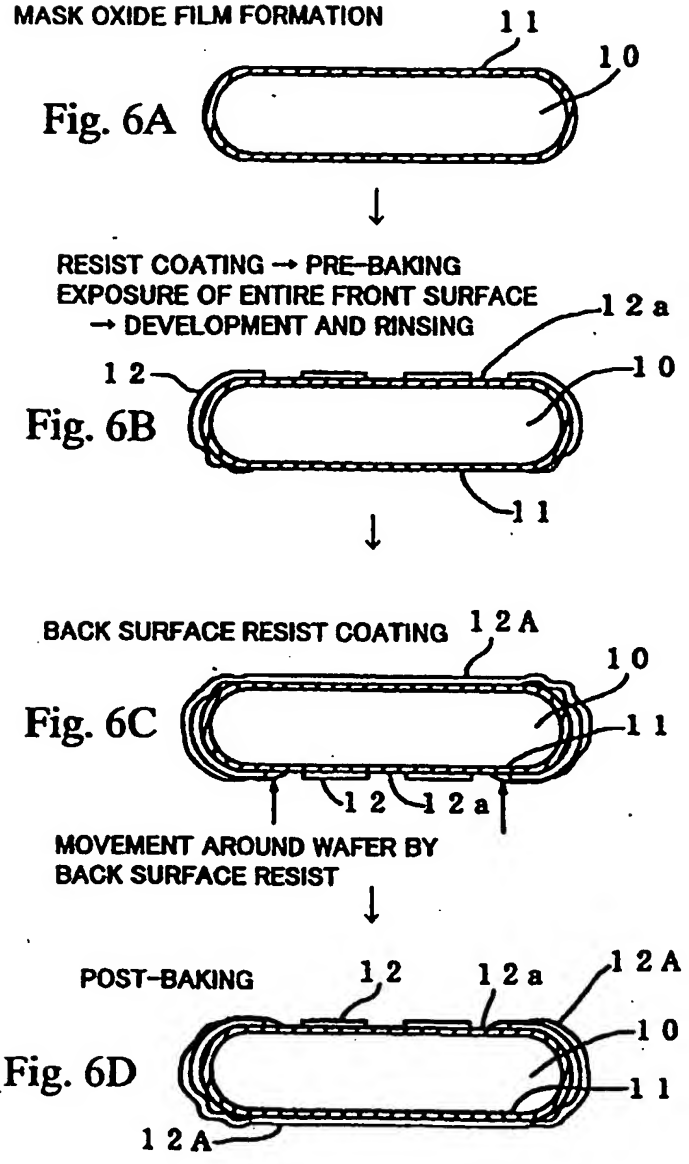


Fig. 6A

Fig. 6B

Fig. 6C

Fig. 6D

MASK OXIDE FILM FORMATION

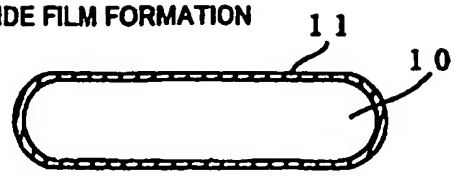


Fig. 7A

RESIST COATING → PRE-BAKING
EXPOSURE OF ENTIRE FRONT SURFACE
→ DEVELOPMENT AND RINSING

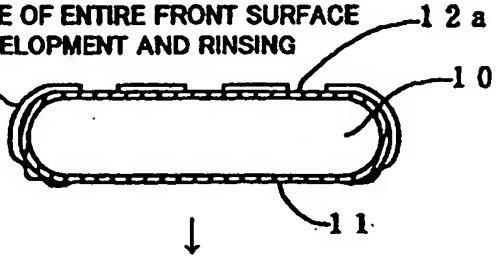


Fig. 7B

BACK SURFACE RESIST COATING

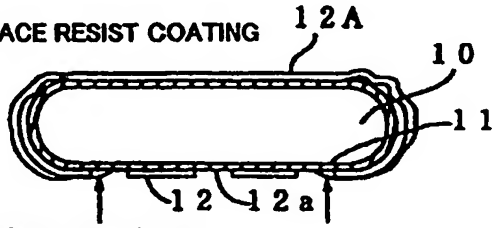


Fig. 7C

MOVEMENT AROUND WAFER BY
BACK SURFACE RESIST

SECOND ROUND OF DEVELOPMENT AND
RINSING FROM FRONT SURFACE

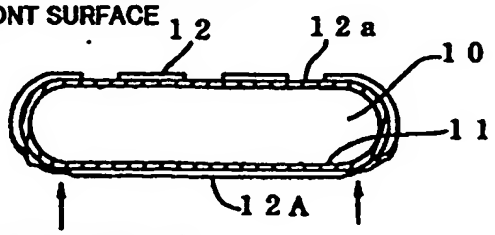


Fig. 7C1

DISSOLVING BY SECOND ROUND OF
DEVELOPING SOLUTION

POST-BAKING

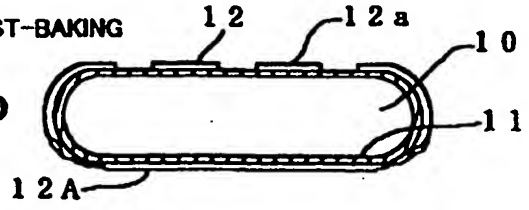
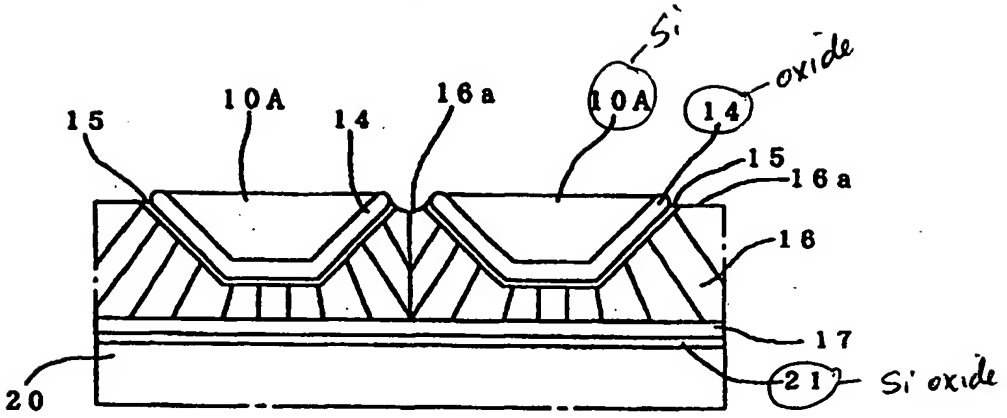


Fig. 7D

Fig. 8



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP99/03297

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[6] H01L21/76

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[6] H01L21/76, H01L21/304, H01L21/306

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Toroku Jitsuyo Shinan Koho 1994-1999
Kokai Jitsuyo Shinan Koho 1971-1999 Jitsuyo Shinan Toroku Koho 1996-1999

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	JP, 05-063071, A (Shin-Etsu Handotai Co., Ltd.), 12 March, 1993 (12. 03. 93), Par. Nos. [0008], [0009] ; Fig. 3 (Family: none)	1-2, 3-6 7-8
Y	JP, 61-191035, A (Rohm Co., Ltd.), 25 August, 1986 (25. 08. 86), Page 1, lower left column, lines 5 to 13 (Family: none)	1-2
Y	JP, 05-082633, A (Hitachi,Ltd.), 2 April, 1993 (02. 04. 93), Par. Nos. [0030] to [0032] ; Figs. 5 to 7 (Family: none)	3-6

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
8 September, 1999 (08. 09. 99)	21 September, 1999 (21. 09. 99)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)